In the Claims:

1. (Original) An arrangement for use in transferring information/structures to wafers using a stamp, the arrangement comprising:

a chuck;

a wafer fixed on the chuck, the wafer being provided with a patterning layer on a main surface thereof; and

a stamp including elevated structures on a main surface, the elevated structures serving as information/structures to be transferred to the patterning layer on the wafer, wherein dimensions of the main surface of the stamp approximately correspond to dimensions of the main surface of the wafer, wherein the stamp is provided with the elevated structures essentially over the entire main surface, and wherein the stamp and the wafer each include mutually assigned pairs of alignment marks such that the stamp can be positioned on the wafer by means of an infrared positioning system and can be pressed into the patterning layer.

2. (Original) The arrangement of claim 1 wherein the alignment marks in the stamp and in the wafer are embodied as buried metal marks.

3. (Original) The arrangement of claim 2 wherein the alignment marks in the stamp are arranged in an edge region of the stamp and wherein the alignment marks in the wafer are arranged in an edge region of the wafer.

4. (Original) The arrangement of claim 1 wherein each pair of alignment marks is assigned an infrared laser situated in the chuck and an infrared camera situated above the stamp.

5. (Original) The arrangement of claim 1 wherein the stamp is fixed to a three-dimensionally positionable stamp mount.

6. (Original) The arrangement of claim 1 wherein the stamp is fixed to a stamp mount that can be positioned two-dimensionally in the X and Y directions, and wherein the chuck is vertically movable.

7. (Original) The arrangement of claim 1 wherein the chuck is provided with an acceptance/transfer device for accepting/transferring the wafer from/to a handler.

8. (Original) The arrangement of claim 7 wherein the acceptance/transfer device comprises at least three pins that extend from the chuck and contact a lower surface of the wafer.

9. (Original) The arrangement of claim 1 wherein the stamp comprises a silicon wafer.

10. (Original) The arrangement of claim 1 wherein the patterning layer comprises a polymer.

11. (Original) The arrangement of claim 1 wherein the patterning layer comprises a resist.

12. (Original) The arrangement of claim 1 wherein the patterning layer comprises a plastically deformable auxiliary patterning layer.

13. (Original) The arrangement of claim 1 wherein the elevated structures comprise structures embedded in the stamp by use of a photolithographic process in conjunction with an etching process.

14-21. (Canceled)

22. (Original) A method of manufacturing a semiconductor wafer, the method comprising:

positioning a semiconductor wafer on a chuck, the semiconductor wafer including alignment marks formed thereon and a patterning layer formed thereon;

positioning a stamp over the semiconductor wafer, the stamp including a plurality of elevated structures disposed on an upper surface thereof and corresponding to a pattern to be applied to the patterning layer of the wafer, the stamp further including alignment marks that correspond to the alignment marks of the semiconductor wafer, the stamp having a diameter dimension that approximately corresponds to a diameter dimension of the semiconductor wafer;

aligning the stamp with the wafer by use of the alignment marks of the semiconductor wafer and of the stamp; and

physically contacting the elevated structures of the stamp with the patterning layer of the semiconductor wafer.

23. (Original) The method of claim 22 wherein the stamp includes elevated structures essentially over the entire upper surface of the stamp.

24. (Original) The method of claim 22 wherein aligning the stamp comprises positioning the stamp on the semiconductor wafer by means of an infrared positioning system.

25. (Original) The method of claim 22 wherein the infrared position system includes a plurality of infrared lasers and a plurality of infrared cameras, wherein each alignment mark on

the stamp is aligned with a corresponding alignment mark on the semiconductor wafer using one of the infrared lasers and one of the infrared cameras.

26. (Original) The method of claim 22 wherein aligning the stamp with the wafer comprises radiating an electromagnetic energy beam in the vicinity of an alignment mark on the wafer and an alignment mark on the stamp and receiving the energy beam at a receiver.

27. (Original) The method of claim 26 wherein the energy beam comprises an infrared light beam.

28. (Original) The method of claim 22 wherein the stamp is fixed to a three-dimensionally positionable stamp mount and wherein aligning the stamp with the wafer comprises moving the stamp while the wafer remains stationary.

29. (Original) The method of claim 22 wherein the stamp is fixed to a stamp mount and wherein aligning the stamp with the wafer comprises moving the stamp two-dimensionally in the X and Y directions and moving the chuck vertically.

30. (Original) The method of claim 22 wherein the chuck is provided with an acceptance/transfer device for accepting/transferring the wafer from/to a handler.

31. (Original) The method of claim 30 wherein the acceptance/transfer device comprises at least three pins that extend from the chuck and contact a lower surface of the wafer.

32. (New) The arrangement according to claim 1 wherein the stamp comprises:

a substrate having a diameter of at least about 200mm;

at least a portion of the elevated structures having a dimension of 0.1 µm or less.

33. (New) The arrangement according to claim 32 wherein at least one feature has a feature size of no greater than 50nm.

34. (New) The arrangement according to claim 1 wherein the stamp comprises buried alignment marks.

35. (New) The arrangement according to claim 34 wherein the alignment marks are arranged in a periphery region of the substrate.

36. (New) The arrangement according to claim 1 wherein the alignment marks are arranged in a periphery region of the substrate.

37. (New) The arrangement according to claim 1 wherein the substrate comprises a silicon wafer.

38. (New) The arrangement according to claim 37 wherein the substrate has a diameter of about or more than 300mm.

39. (New) The arrangement according to claim 2 wherein the alignment marks are arranged in a periphery region of the substrate.